

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendment can be found in the specification, for example, on page 10 lines 4-9 and FIG. 3, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-19 under 35 U.S.C. §103(a) as being unpatentable over Chan et al. '505 (hereafter Chan) in view of Rangasayee '225 is respectfully traversed and should be withdrawn.

Chan concerns a hybrid routing architecture for high density complex programmable logic devices (Title). Rangasayee concerns an integrated circuit incorporating a programmable cross-bar switch (Title). In contrast, claim 1 provides (in part) an assembly apparatus mounting a programmable logic device (PLD) and a die. The Office Action asserts on page 2 that a CPLD 100 in FIG. 2 of Chan is similar to the claimed assembly apparatus. However, no explanation or evidence is provided why one of ordinary skill in the art would consider a CPLD to be an assembly apparatus.

Therefore, *prime facie* obviousness has not been established for lack of evidence of each claimed element.

Furthermore, the Office Action asserts on page 2 that the CPLD of Chan is similar to the claimed PLD. However, Chan appears to be silent regarding the CPLD being mounted on itself as asserted in the Office Action. Furthermore, both Chan and Rangasayee appear to be silent regarding mounting another CPLD from Rangasayee on the CPLD of Chan (asserted similar to the claimed assembly apparatus). Therefore, Chan and Rangasayee, alone or in combination, do not appear to teach or suggest an assembly apparatus mounting a PLD and a die as presently claimed.

Claim 1 further provides a first communication channel of the die coupled to a first of a plurality of routing channels of the PLD to exchange a first parallel data signal with at least one of a plurality of logic block clusters in the PLD. In contrast, both Chan and Rangasayee appear to be silent regarding coupling the routing channels in the CPLD of Chan with the horizontal conductors 178 (parallel interface of the row I/O block 164, asserted to be similar to the claimed first communication channel) in FIG. 8 of Rangasayee. In addition, the Office Action and references are silent regarding coupling the routing channels in the CPLD of Chan with the row I/O block 164 of Rangasayee. Therefore, Chan and Rangasayee, alone or in combination, do not appear to teach or suggest a first communication channel of a die coupled to a first

of a plurality of routing channels of a PLD to exchange a first parallel data signal with at least one of a plurality of logic block clusters in the PLD as presently claimed.

Furthermore, the Office Action has not provided clear and particular evidence of motivation to combine the references. In particular, the asserted motivation on page 3 of the Office Action "to increase flexibility enables the CPLD to fit more complex logic functions more often than possible with conventional CPLD architectures" appears to be motivation to implement the architecture taught by Rangasayee in the design of the CPLD from Chan. However, the asserted motivation does not appear to explain why one of ordinary skill in the art would be motivated to mount the CPLD of Rangasayee and the CPLD of Chan on the same assembly apparatus and connect the horizontal conductors 178 of Rangasayee with the routing channels of Chan. Therefore, *prima facie* obviousness has not been established for lack of evidence of motivation to combine the references.

Furthermore, Rangasayee appears to be silent regarding the horizontal conductors 178 being accessible outside the CPLD of Rangasayee. Coupling a first communication channel of a die to a routing channel of a PLD does not appear to be possible between Chan and Rangasayee. Therefore, *prima facie* obviousness has not been established for a lack of showing for a reasonable expectation of success for the proposed combination. Claims 11 and 19 provide

language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 2 provides (from claim 1) a first communication channel in a die configured to convert between a first serial data signal and a first parallel data signal and (from claim 2) a second communication channel in the die configured to convert between a second serial data signal and a second parallel data signal. In contrast, FIG. 8 and the associated text on column 8, lines 13-28 of Rangasayee, cited on page 3 of the Office Action, appear to be silent regarding two communication channels converting two serial signals into two parallel signals. Therefore, Chan and Rangasayee, alone or in combination, do not appear to teach or suggest a first communication channel in a die configured to convert between a first serial data signal and a first parallel data signal and a second communication channel in the die configured to convert between a second serial data signal and a second parallel data signal as presently claimed. Claims 10 and 12 provide similar language to claim 2 as discussed above.

Claim 2 further provides the second communication channel in the die is coupled to a second routing channel of the PLD. In contrast, both Chan and Rangasayee appear to be silent regarding coupling conductors inside the CPLD of Rangasayee with the routing channels inside the CPLD of Chan. Therefore, Chan and Rangasayee,

alone or in combination, do not appear to teach or suggest a second communication channel in a die coupled to a second routing channel of a PLD as presently claimed. Claim 12 also provides language similar to claim 2 as discussed above. As such, claims 2, 10 and 12 are fully patentable over the cited references and the rejection should be withdrawn.

Claims 3 and 13 provide three communication channels in the die coupled to three routing channels in the PLD. As argued above for claims 2 and 12, both Chan and Rangasayee, alone or in combination, do not appear to teach or suggest (i) multiple communications channels and (ii) coupling the multiple communications channels to multiple routing channels. As such, claims 3 and 13 are fully patentable over the cited references and the rejection should be withdrawn.

Claims 4 and 14 provide four communication channels in the die coupled to four routing channels in the PLD. As argued above for claims 2 and 12, both Chan and Rangasayee, alone or in combination, do not appear to teach or suggest (i) multiple communications channels and (ii) coupling the multiple communications channels to multiple routing channels. As such, claims 4 and 14 are fully patentable over the cited references and the rejection should be withdrawn.

Claims 5, 15 and 18 provide two communications channels in the die coupled to a first routing channel in the PLD. In

contrast, both Chan and Rangasayee appear to be silent regarding (i) multiple communications channels and (ii) coupling the multiple communications channels to a single routing channel. Therefore, Chan and Rangasayee, alone or in combination, do not appear to teach or suggest two communications channels in a die coupled to a first routing channel in a PLD as presently claimed. As such, claims 5, 15 and 18 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 6 provides the first communication channel in the die receiving a control signal from one of a plurality of logic block clusters in the PLD. Page 4 of the Office Action cites column 7, lines 25-44 of Chan as teaching an output signal from the routing channels. However, Rangasayee appears to be silent regarding the row I/O block 164 (asserted similar to the claimed first communication channel) being capable of receiving such a control signal from outside the CPLD via the horizontal conductors 178. Therefore, Chan and Rangasayee, alone or in combination, do not appear to teach or suggest a first communication channel in a die receiving a control signal from one of a plurality of logic block clusters in a PLD as presently claimed. Claims 8, 16 and 17 provides language similar to claim 6. As such, claims 6, 8, 16 and 17 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 7 provides that the control signal is an encoding selection signal. In contrast, both Chan and Rangasayee appear to be silent regarding an encoding selection signal. Therefore, Chan and Rangasayee, alone or in combination, do not appear to teach or suggest an encoding selection signal as presently claimed.

Claim 9 provides a status signal configured as a special character indicator. In contrast, both Chan and Rangasayee appear to be silent regarding a special character indicator. Therefore, Chan and Rangasayee, alone or in combination, do not appear to teach or suggest a status signal configured as a special character indicator as presently claimed. As such, claim 9 is fully patentable over the cited references and the rejection should be withdrawn.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicants' representative respectfully requests any further action on the merits be presented as a non-final action. 37 CFR §1.104(b) states:

(b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

Claim 20 was not addressed by the Office Action. As such, the Office Action mailed May 20, 2004 is not complete.

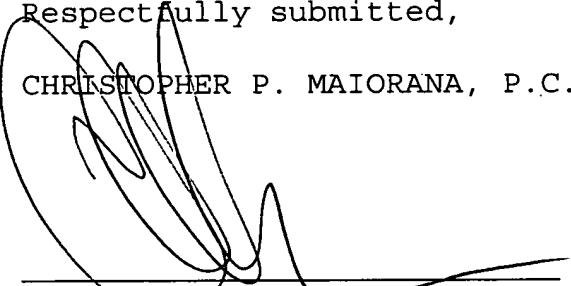
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
Registration No. 42,829
24840 Harper Avenue, Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

Dated: August 3, 2004

Docket No.: 0325.0485